ABSTRACT

A cell transistor of a flash memory device includes a semiconductor substrate, a source region, a drain region, a floating gate, an inter-gate insulating layer, and a control gate, wherein the floating gate has a tip protruding into an end portion of the source region. With the application of erasing voltages to the source region and the control gate, an intense electric field is induced on the tip of the floating gate. Accordingly, an erasing efficiency of the cell transistor can be enhanced.